**Lab Number: 8**

**Section Number: 001**

**Names: Barak Barclay**

**Assigned Date: 04/07/2016**

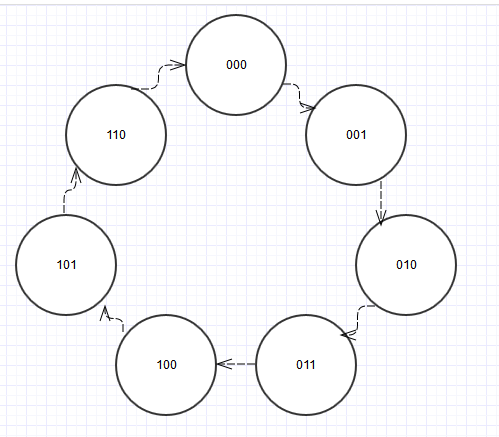
**Due Date: 04/14/2016 (Due date extended to 04/15 because of being sick.)**

**Introduction:**

In this lab, a state diagram, a transition table, all necessary Karnaugh maps, a Logisim schematic, and a Behavioral Model Verilog program will be created for a 3 bit counter that counts from 000 to 110 and starts on an input pulse.

**Part 1:**

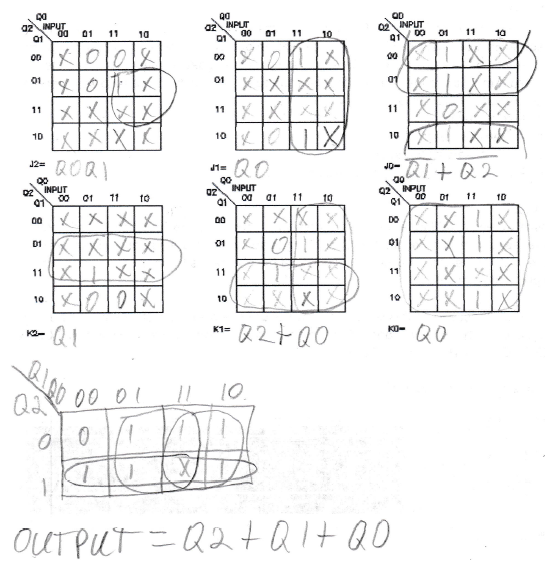
***Part 1 A.)***



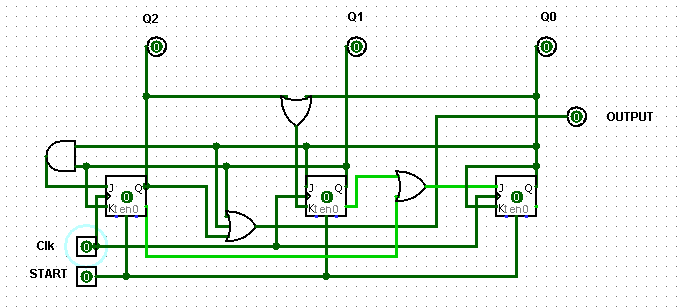
***Part 1 B.)***

******

***Part 1 C.)***



***Part 1 D.)***



**Part 2:**

// 3 bit counter from 000 to 110 that starts on an input pulse

module L8(output Q2,Q1,Q0,OUTPUT, output [2:0]State, input START,clock,reset);

reg[2:0]state;

assign OUTPUT=Q2||Q1||Q0;

parameter S0=3'b000, S1=3'b001, S2=3'b010, S3=3'b011, S4=3'b100, S5=3'b101, S6=3'b110;

always @(posedge clock or negedge reset)

if(reset==0) state <=S0;

else case (state)

S0: if(START) state=S1;

S1: if(START) state=S2;

S2: if(START) state=S3;

S3: if(START) state=S4;

S4: if(START) state=S5;

S5: if(START) state=S6;

S6: if(START) state=S0;

endcase

assign Q2=state[2];

assign Q1=state[1];

assign Q0=state[0];

assign State[2]=state[2];

assign State[1]=state[1];

assign State[0]=state[0];

endmodule

// 3 bit counter from 000 to 110 that starts on an input pulse test bench

module L8TB;

wire Q2,Q1,Q0,OUTPUT;

wire [2:0]State;

reg START,clock,reset;

L8 M1(Q2,Q1,Q0,OUTPUT,State,START,clock,reset);

initial

begin

$monitor ("Q2Q1Q0=%b%b%b OUTPUT=%b", Q2,Q1,Q0,OUTPUT);

START = 1'b0;clock = 1'b0;reset = 1'b0;

#5 START = 1'b0;clock = 1'b0;reset = 1'b1;

#5 START = 1'b0;clock = 1'b1;reset = 1'b1;

#10 START = 1'b0;clock = 1'b0;reset = 1'b1;

forever begin

#10 START = 1'b1;clock = 1'b1;reset = 1'b1;

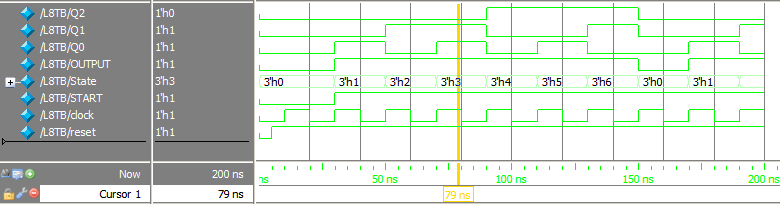
#10 START = 1'b1;clock = 1'b0;reset = 1'b1;

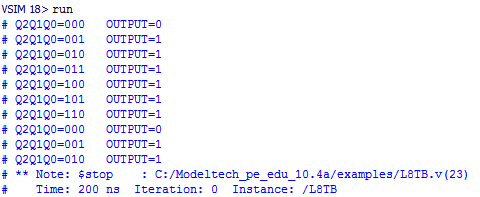
end

end

initial #200 $stop;

endmodule





**Conclusion:**

The state diagram was created using <https://www.gliffy.com/go/html5/launch?app=1b5094b0-6042-11e2-bcfd-0800200c9a66>. The transition table was created using the state diagram and a modified function table for a JK flip-flop. The Karnaugh maps were created using the transition table. The Logisim schematic was created using the equations derived from the Karnaugh maps.

The Behavioral Model Verilog program was created by modifying the 2-bit up/down counter Behavioral Model Verilog program from last lab. Outputs A and B were replaced by Q2,Q1,Q0 and OUTPUT. The dir input was replaced with the START input. Output was assigned Q2 OR Q1 OR Q0. Additional states were added. The test bench was modified to re-create the wave asked for.